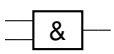
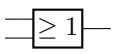
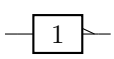
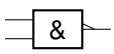
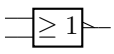
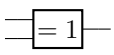
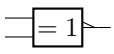
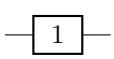
Logic Gate Symbols — One-Page Cheat Sheet

ANSI/IEEE Std 91-1984 distinctive shapes vs. IEC 60617-12 rectangular shapes · truth tables · Boolean expressions · 74xx / 4000 parts

Gate	ANSI/IEEE (distinctive)	IEC (rectangular)	Boolean expression	Y for AB = 00 01 10 11	Output rule
AND			$Y = A \cdot B$	0 0 0 1	HIGH only if *all* inputs HIGH
OR			$Y = A + B$	0 1 1 1	HIGH if *any* input HIGH
NOT			$Y = \overline{A}$	* * *	Inverts the single input
NAND			$Y = \overline{A \cdot B}$	1 1 1 0	LOW only if *all* inputs HIGH
NOR			$Y = \overline{A + B}$	1 0 0 0	HIGH only if *all* inputs LOW
XOR			$Y = A \oplus B$	0 1 1 0	HIGH if inputs *differ*
XNOR			$Y = \overline{A \oplus B}$	1 0 0 1	HIGH if inputs *match*
Buffer			$Y = A$	* * *	Passes input, restores drive

* NOT and Buffer are single-input

Reading Any Gate Symbol

The bubble is the whole trick. A small circle means logical inversion at that point.

Where	Meaning
On the output	Invert the result: AND → NAND, OR → NOR
On an input	That input is active LOW
None	Plain active-HIGH gate

Note: A NAND drawn with bubbles on both *inputs* and no output bubble is still an OR gate. That is De Morgan's theorem, $\overline{A} + \overline{B} = \overline{A \cdot B}$, drawn as a symbol. Both forms are legal and mean the same circuit.

IEC qualifying symbols (inside the rectangle):

Sym	Gate	Sym	Gate
&	AND / NAND	1	Buffer / NOT
≥1	OR / NOR	=1	XOR

Pin convention: inputs on the left (A, B), output on the right (Y). Power pins (V_{CC}, GND) are almost never drawn on the gate symbol — they live in a separate power symbol or the netlist.

Symbol to Real Part: 74xx & 4000 Series

Gate	74HC part	4000 part	Gates/pkg
AND	74HC08	CD4081	4
OR	74HC32	CD4071	4
NOT	74HC04	CD4069	6
NAND	74HC00	CD4011	4
NOR	74HC02	CD4001	4
XOR	74HC86	CD4070	4
XNOR	74HC266†	CD4077	4
Buffer	74HC4050	CD4050	6

† 74HC266 has open-drain outputs and needs a pull-up resistor.

Note: One symbol ≠ one part. A quad NAND puts four gates in one DIP-14 or SOIC-14 package, so four NAND symbols scattered across your schematic can all resolve to a single 74HC00. Tie every unused input HIGH or LOW — never leave a CMOS input floating.

Universal Gates: Build Anything

Target	NAND gates	NOR gates
NOT	1 (tie inputs together)	1 (tie inputs together)
AND	2	3
OR	3	2
NAND	—	4
NOR	4	—
XOR	4	5

Common traps: Missing the output bubble (AND read as NAND is the single most common schematic misread) · Assuming IEC 1 means logic HIGH — it is the buffer qualifier · Reading XOR as OR at small zoom (look for the second curved input line) · Forgetting that the schematic symbol carries no package information; the footprint decides the land pattern.

Reference: ANSI/IEEE Std 91-1984 (distinctive shapes) · IEC 60617-12 (rectangular shapes) · MIL-STD-806 (historical origin of the distinctive shapes).